

## 3.3V Low Skew 1-to-4 Differential/LVCMOS to LVPECL Fanout Buffer

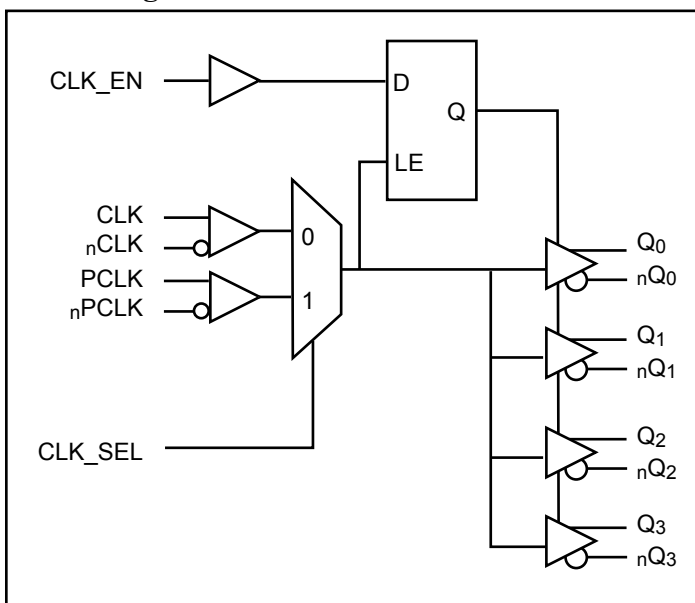
### Features

- Pin-to-pin compatible to ICS8533-01
- Maximum operation frequency: 800MHz
- 4 pair of differential LVPECL outputs
- Selectable differential CLK and PCLK inputs
- CLK, nCLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- PCLK, nPCLK pair supports LVPECL, CML and SSTL input level
- Output Skew: 100ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V power supply
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green available):  
-20-pin TSSOP (L)

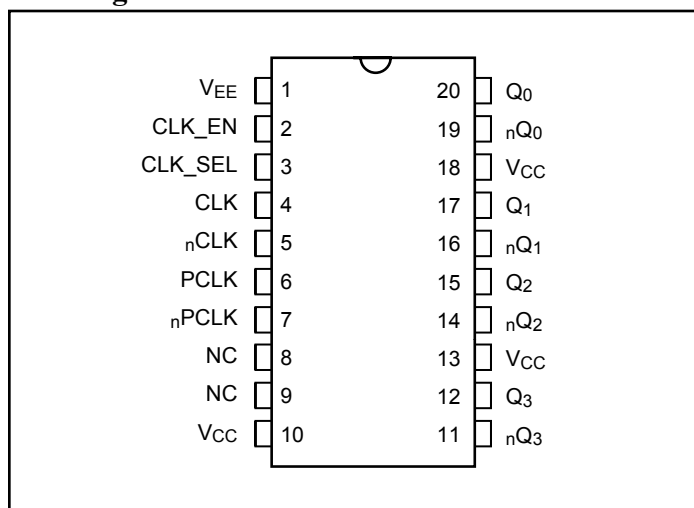
### Description

The PI6C48533-01 is a high-performance low-skew LVPECL fanout buffer. PI6C48533-01 features two selectable differential inputs and translates to four LVPECL ultra-low jitter outputs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LPECL or LVDS or LVHSTL or SSTL or HCSL signals, and PCLK input accepts LVPECL or SSTL or CML signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK\_EN pin. PI6C48533-01 is ideal for differential to LVPECL translations and/or LVPECL clock distribution. Typical clock translation and distribution applications are data-communications and telecommunications.

### Block Diagram



### Pin Diagram



### Pin Description

Name	Pin #	Type	Description
V <sub>EE</sub>	1	P	Connect to Negative power supply
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Q <sub>x</sub> outputs are forced low, <sub>n</sub> Q <sub>x</sub> outputs are forced high. LVCMOS/LVTTL level with 50KΩ pull-up.
CLK_SEL	3	I_PD	Clock select input. When high, selects PCLK input. When low, selects CLK input. LVCMOS/LVTTL level with 50KΩ pull-down.
CLK	4	I_PD	Non-inverting differential clock input
<sub>n</sub> CLK	5	I_PU	Inverting differential clock input
PCLK	6	I_PD	Non-inverting differential clock input
<sub>n</sub> PCLK	7	I_PU	Inverting differential clock input
NC	8, 9		Not connected
V <sub>CC</sub>	10, 13, 18	P	Connect to 3.3V.
Q <sub>3</sub> , <sub>n</sub> Q <sub>3</sub>	11, 12	O	Differential output pair, LVPECL interface level.
Q <sub>2</sub> , <sub>n</sub> Q <sub>2</sub>	14, 15	O	Differential output pair, LVPECL interface level.
Q <sub>1</sub> , <sub>n</sub> Q <sub>1</sub>	16, 17	O	Differential output pair, LVPECL interface level.
Q <sub>0</sub> , <sub>n</sub> Q <sub>0</sub>	19, 20	O	Differential output pair, LVPECL interface level.

**Note:**

1. I = Input, O = Output, P = Power supply connection, I\_PD = Input with pull down, I\_PU = Input with pull up

### Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance				4	pF
R <sub>pullup</sub>	Input Pullup Resistance			50		KΩ
R <sub>pulldown</sub>	Input Pulldown Resistance			50		

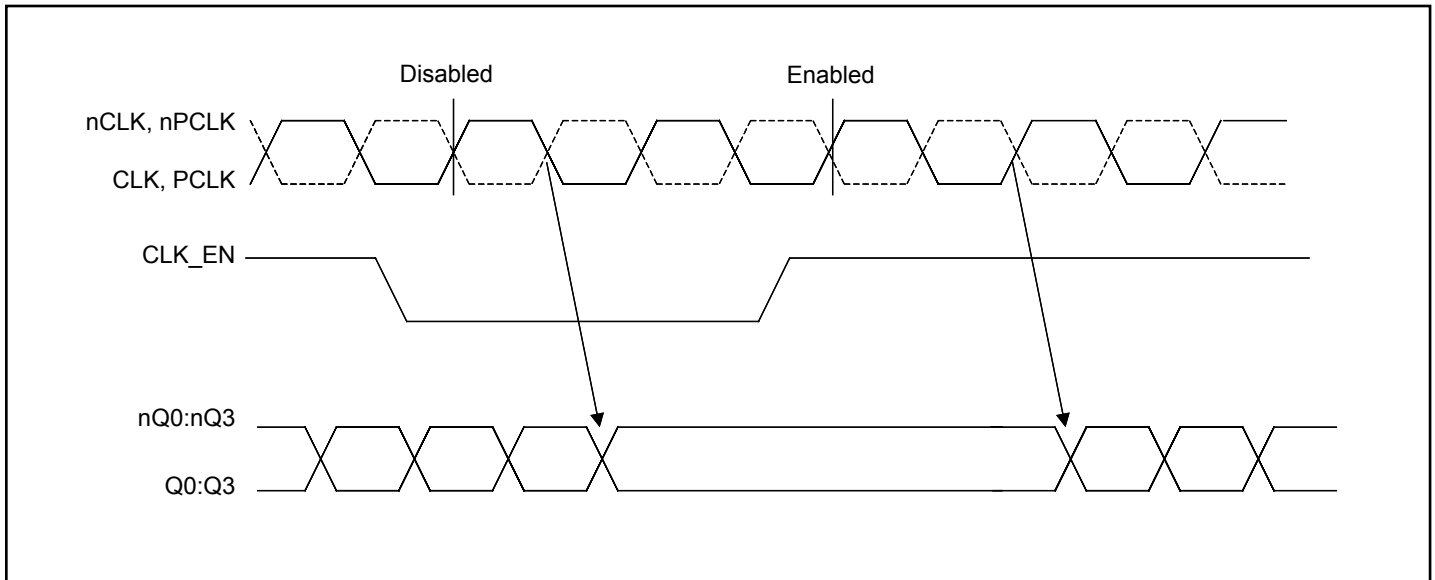
### Control Input Function Table<sup>(1)</sup>

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q <sub>0</sub> :Q <sub>3</sub>	<sub>n</sub> Q <sub>0</sub> : <sub>n</sub> Q <sub>3</sub>
0	0	CLK, <sub>n</sub> CLK	Diased: Low	Diased: High
0	1	PCLK, <sub>n</sub> PCLK	Disabled: Low	Disabled: High
1	0	CLK, <sub>n</sub> CLK	Enabled	Enabled
1	1	PCLK, <sub>n</sub> PCLK	Enabled	Enabled

**Note:**

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

**Figure 1. CLK\_EN Timing Diagram**



**Clock Input Function Table**

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	nCLK or nPCLK	Q0:Q3	nQ0:nQ3		
0	1	LOW	HIGH	Differential to Differential	None Inverting
1	0	HIGH	LOW	Differential to Differential	None Inverting
0	Biased; $V_{IN} = V_{CC}/2$	LOW	HIGH	Single Ended to Differential	None Inverting
1	Biased; $V_{IN} = V_{CC}/2$	HIGH	LOW	Single Ended to Differential	None Inverting
$V_{CC}/2$	0	HIGH	LOW	Single Ended to Differential	Inverting
$V_{CC}/2$	1	LOW	HIGH	Single Ended to Differential	Inverting

**Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{CC}$	Supply voltage	Referenced to GND			4.6	V
$V_{IN}$	Input voltage	Referenced to GND	-0.5		$V_{CC}+0.5V$	
$V_{OUT}$	Output voltage	Referenced to GND	-0.5		$V_{CC}+0.5V$	
$T_{STG}$	Storage temperature		-65		150	°C

**Note:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>CC</sub>	Power Supply Voltage		3.0	3.3	3.6	V
T <sub>A</sub>	Ambient Temperature		-40		85	°C
I <sub>EE</sub>	Power Supply Current	500 MHz			60	mA

### LVCMOS/LVTTL DC Characteristics (T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 3.0V to 3.6V unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input High Voltage		2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	
I <sub>IH</sub>	Input High Current	CLK, CLK_SEL	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		150	μA
		CLK_EN	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		5	
I <sub>IL</sub>	Input Low Current	CLK, CLK_SEL	V <sub>IN</sub> = 0V, V <sub>CC</sub> = 3.6V	-5		
		CLK_EN	V <sub>IN</sub> = 0V, V <sub>CC</sub> = 3.6V	-150		

### Differential DC Input Characteristics (T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 3.0V to 3.6V unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I <sub>IH</sub>	Input High Current	nCLK, nPCLK	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		5	μA
		CLK, PCLK	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		150	μA
I <sub>IL</sub>	Input Low Current	nCLK, nPCLK	V <sub>CC</sub> = 3.6V, V <sub>IN</sub> = 0V	-150		μA
		CLK, PCLK	V <sub>CC</sub> = 3.6V, V <sub>IN</sub> = 0V	-5		μA
V <sub>PP</sub>	Peak-to-peak Voltage		0.15		1.3	V
V <sub>CMR</sub>	Common Mode Input Voltage <sup>(1, 2)</sup>		V <sub>EE</sub> +0.5		V <sub>CC</sub> -0.85V	V

#### Notes:

1. For single ended applications, the maximum input voltage for CLK and nCLK is V<sub>CC</sub>+0.3V
2. Common mode voltage is defined as V<sub>IH</sub>.

### LVPECL DC Characteristics

( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.0\text{V}$  to  $3.6\text{V}$ ,  $R_L = 50\Omega$  to  $V_{CC} - 2\text{V}$ , unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{IH}$	Input High Current	$n\text{CLK}, n\text{PCLK}$	$V_{IN} = V_{CC} = 3.6\text{V}$		5	$\mu\text{A}$
		CLK, PCLK	$V_{IN} = V_{CC} = 3.6\text{V}$		150	
$I_{IL}$	Input Low Current	$n\text{CLK}, n\text{PCLK}$	$V_{CC} = 3.6\text{V}, V_{IN} = 0\text{V}$	-150		
		CLK, PCLK	$V_{CC} = 3.6\text{V}, V_{IN} = 0\text{V}$	-5		
$V_{PP}$	Peak-to-peak Voltage		0.3		1	V
$V_{CMR}$	Common Mode Input Voltage; Note <sup>(1,2)</sup>		$V_{EE}+1.5$		$V_{CC}$	
$V_{OH}$	Output High Voltage		$V_{CC}-1.4$		$V_{CC}-0.9$	
$V_{OL}$	Output Low Voltage		$V_{CC}-2.0$		$V_{CC}-1.6$	
$V_{SWING}$	Peak-to-peak Output Voltage Swing		0.6		1.0	

#### Notes:

- For single ended applications, the maximum input voltage for PCLK and  $n\text{PCLK}$  is  $V_{CC}+0.3\text{V}$ .
- Common mode voltage is defined as  $V_{IH}$ .

### AC Characteristics<sup>(1)</sup> ( $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ , $V_{CC} = 3.0\text{V}$ to $3.6\text{V}$ , $R_L = 50\Omega$ to $V_{CC} - 2\text{V}$ , unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{max}$	Output Frequency			500	800	MHz
$t_{pd}$	Propagation Delay <sup>(2)</sup>		1.0		2.0	ns
Tsk(o)	Output-to-output Skew <sup>(3)</sup>				100	ps
Tsk(pp)	Part-to-part Skew <sup>(4)</sup>				150	
$t_r/t_f$	Output Rise/Fall time	20% - 80%	75		300	
odc	Output duty cycle		40		60	%

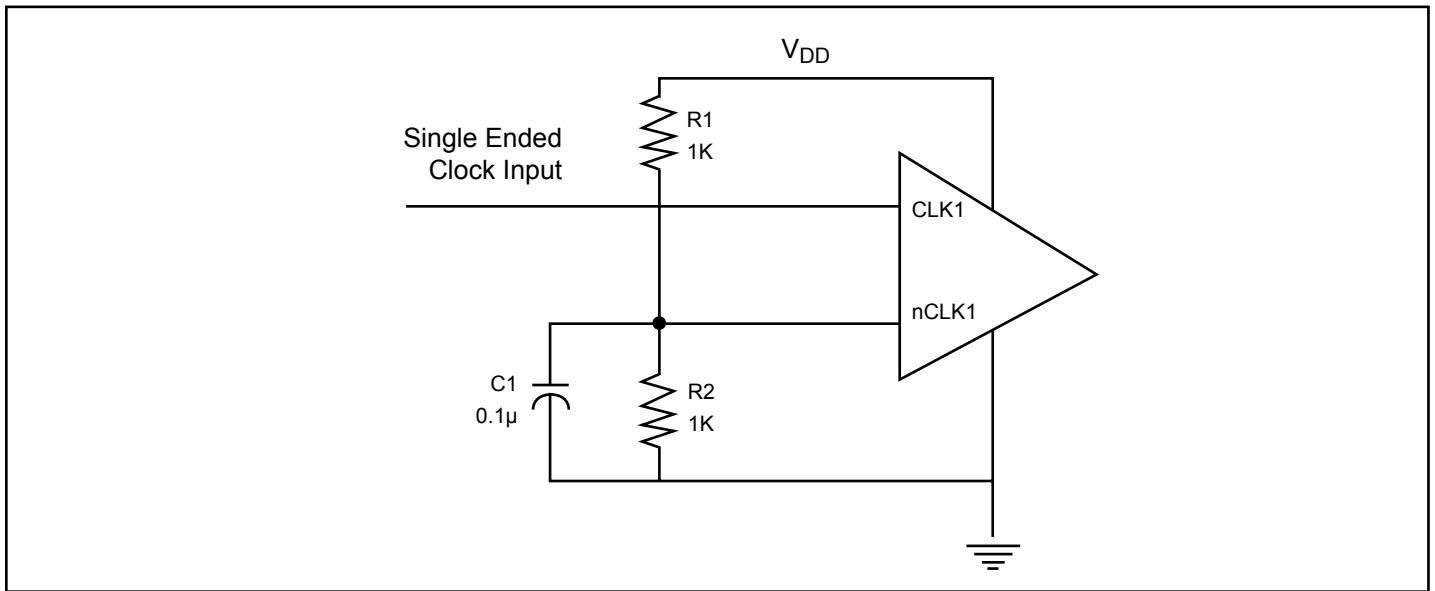
#### Notes:

- All parameters are measured at 500MHz unless noted otherwise
- Measured from the  $V_{CC}/2$  of the input to the differential output crossing point
- Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
- Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.

### Applications Information

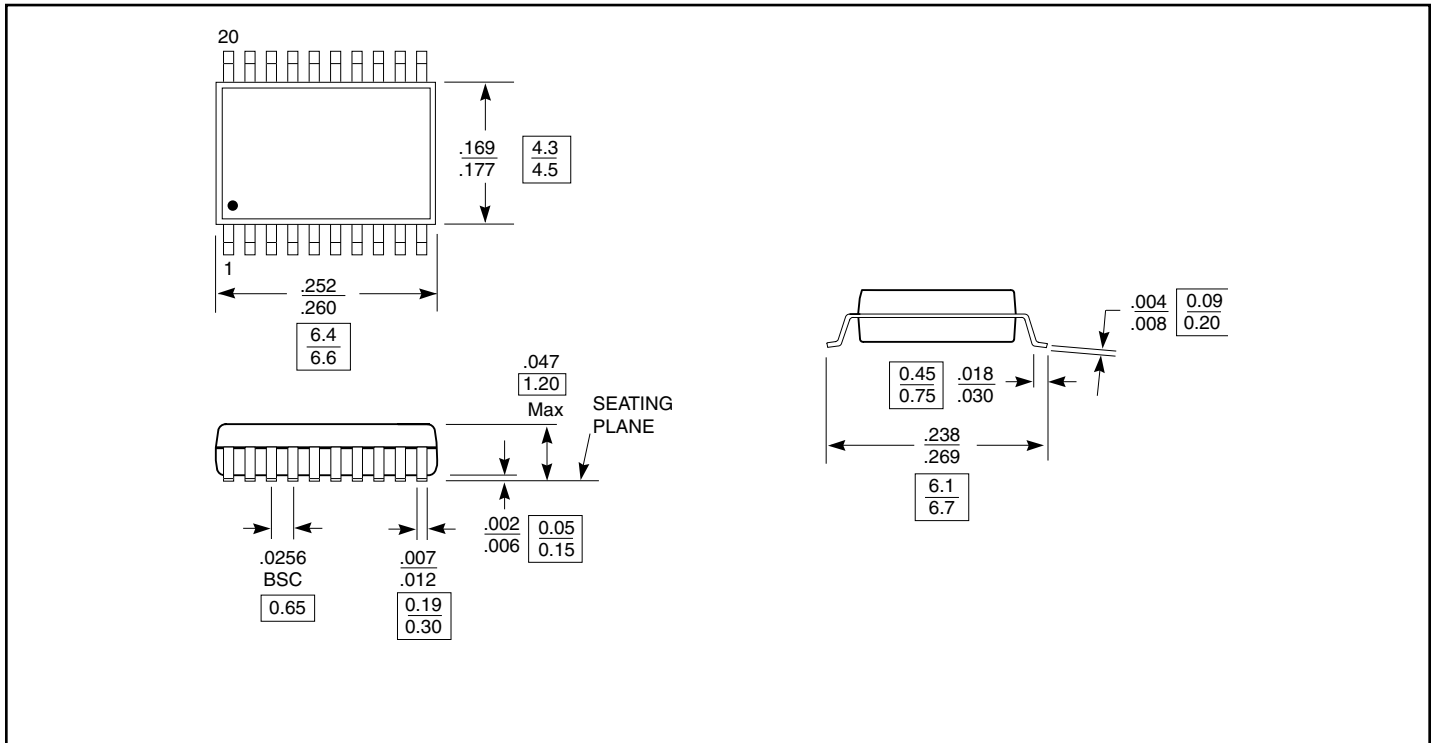
#### *Wiring the differential input to accept single ended levels*

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .



**Figure 2: Single-ended Signal Driving Differential Input**

**Packaging Mechanical: 20-Pin TSSOP (L)**



**Ordering Information(1,2)**

Ordering Code	Package Code	Package Description
PI6C48533-01LE	L	Pb-free & Green 20-pin 173-mil wide TSSOP

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green